CIS 310 Operating Systems

Week 10: Virtual *Memory*

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Friday 5th November, 2021

Outline

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- Trap to the OS. *k-stack* saved to current (parent) PCB.
- Duplicate parent PCB, duplicate all FD, duplicate memory assignment but separate writable pages.
- **Policy** Prefer parent or child process by returning from the system call to one or the other.

`exec("cmd")`

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  Will read from *filesystem*. Will modify *context*. Privileged operations.
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- Modify context so `IP` contains the virtual starting address for a new program.
- Return from interrupt.

Address Space

Definition

An address space is *all* of the memory that a (process/machine) can **address**.

- If the addresses refer to actual RAM locations, they are **physical** addresses in a physical address space.
- If the addresses must be translated before they refer to actual RAM locations, they are **virtual** addresses in a virtual address space.

The *size* of an address space is determined by the number of address bits it has: *n* **bits** of address $\Rightarrow 2^n$ **bytes** of memory.

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- Indirect addressing, through an OS-supported translator, is always applied for user-space machine code.

Address Translation

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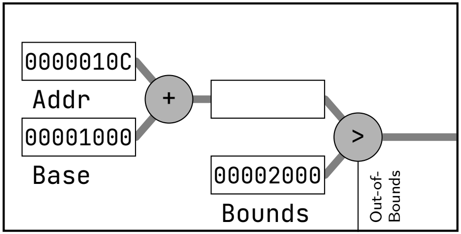
- The base register alone can permit user programs to generate dangerous addresses.
- Combined with a **bounds register**, the translation is much safer.

Memory Management Unit

Fetch

IP	0000010C
Base	00001000
Bounds	00002000



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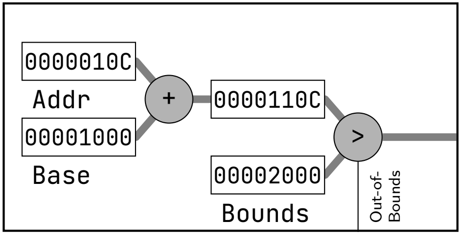
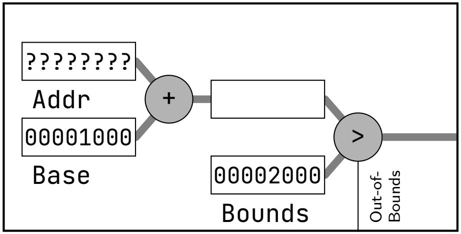


Memory Management Unit

```
load R1, 0x00001100
 Base     00001000
 Bounds   00002000
```



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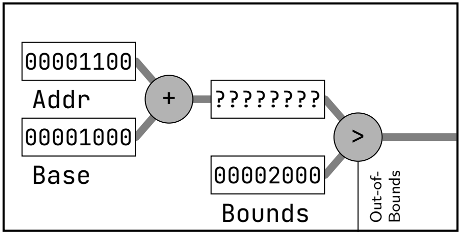

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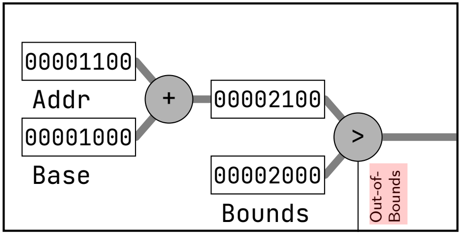

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- Fixed size process spaces will probably over allocate for many processes, wasting memory in *internal* fragmentation.
- Variable-size process spaces will lead to *external* fragmentation.

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- **Speed**: Another problem is speed of addition. $O(\log(\text{bits}))$

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- Small *page size* with translation information accessed indirectly from RAM is **paged virtual memory**.

Address Translation

Page Table

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`<page #>`	`<offset>`

  Only the *page #* is translated from the virtual to the physical address.

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- The *offset* is a fixed number of bits wide so that the bounds register is no longer required.

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- Use `page` as an index into the page table array
- Get `frame` out of page table entry
- Combine `<frame,offset>` into *physical address*

Page Lookup

Fetch

Page Size	`4KB`
`IP`	`0000210C`
`PTBR`	`F0000000`
`sizeof``(PTE)`	`4B`

Offset Bits:

Page Lookup

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Page Size	`4KB`
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Offset Bits: `12b`

Page #:

Page Lookup

Fetch

Page Size	4KB
IP	0000210C
PTBR	F0000000
sizeof(PTE)	4B

Offset Bits: 12b

Page #: 00002

Offset:

Page Lookup

Fetch

Page Size	`4KB`
IP	`0000210C`
PTBR	`F0000000`
`sizeof``(PTE)`	`4B`

Offset Bits: `12b`

Page #: `00002`

Offset: `10C`

Address of PTE:

Page Lookup

Fetch

Page Size	`4KB`
`IP`	`0000210C`
`PTBR`	`F0000000`
`**sizeof**(PTE)`	`4B`

Offset Bits: `12b`

Page #: `00002`

Offset: `10C`

Address of PTE: `F0000000` +

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Page #: `00002`

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Address of PTE: `F0000000` $+$ `4` $\times$

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Address of PTE: F0000000 $+$ 4 $\times$ 00002 $=$

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Offset Bits: `12b`

Page #: `00002`

Offset: `10C`

Address of PTE: `F0000000` $+$ `4` $\times$ `00002` $=$ `F0000008`

`RAM[F0000008] = 007F2`

Page Lookup

Fetch

Page Size	`4KB`
IP	`0000210C`
PTBR	`F0000000`
`sizeof``(PTE)`	`4B`

Offset Bits: `12b`

Page #: `00002`

Offset: `10C`

Address of PTE: `F0000000` $+$ `4` $\times$ `00002` $=$ `F0000008`

`RAM[F0000008] = 007F2`

Physical Address:

Page Lookup

Fetch

Page Size	4KB
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PTBR	`F0000000`
`sizeof``(PTE)`	4B

Offset Bits: 12b

Page #: `00002`

Offset: `10C`

Address of PTE: $\texttt{F0000000} + 4 \times \texttt{00002} = \texttt{F0000008}$

`RAM[F0000008] = 007F2`

Physical Address: `007F210C`

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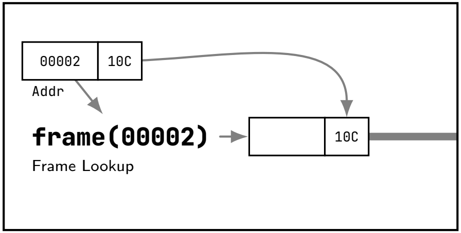

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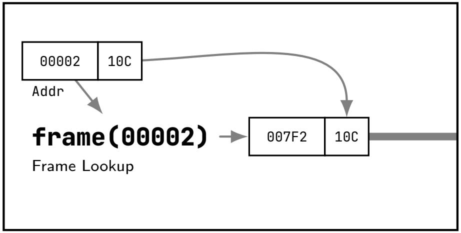
00002
10C
Addr
frame(00002)
Frame Lookup
007F2
10C